Experiment No. 04:

Memory Design Using Static Random Access Memory

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ECE 441-001

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Acknowledgment: I acknowledge all of the work (including figures and codes) belongs to me and/or persons who are referenced.

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**I. Introduction**

**A. Purpose**

The purpose of this lab is to help students understand the concept of memory design and implementing it using a breadboard, components and the SANPER-1’s data bus. Having a knowledge of memory table is also essential for this lab.

**B. Background**

Memory is vital in computer design since most programs, including the operating system of a computer, are stored in memory. In this lab, students are required to design a memory access unit using 4 static RAM chips. Note that SRAM was used instead of DRAM. Although SRAM is more expensive, it offers a better performance than DRAM and reads/write more rapidly. The students were asked to design a proper logic to access odd and even address lines. The address lines need to be accessed when the address strobe is asserted. UDS and LDS signals can be useful to decode odd and even bytes. After accessing the memory, since the access time of SRAM is slower the clock speed of the microprocessor, a delay logic has to be implemented to assert the DTACK signal and allow operations between the microprocessor and the memory design to occur. Students had to allocate memory space to their memory design which would not affect the existing components. This group chose address range: $8B800-$8BFFF since it was free. For this address range, the students used A15,A11 and A13 as the input to the decoder and used the output 7 to transfer data to their memory design.

**II. Lab Procedure and Equipment List**

**A. Equipment**

*Equipment*

* SANPER-1 system
* PC with TUTOR software
* Breadboard
* ECE 441 Lab Kit (includes 74LS138, 74LS74, 74LS02, 74LS04, 74LS05, and different valued resistors)

**B. Procedure**

1. Implement the schematic designed on the breadboard.
2. Connect the hardware to the SANPER-1 ELU.
3. Execute the memory test from the program designed in the preliminary assignment.

**III. Results and Analysis**

When testing the code, the memory design could successfully read and write from the memory. However, one of the SRAM chips was not working properly which caused some issues with the data transfer.

1. **Discussion**

Programs

ORG $800

MSGPASS DC.B 'MEMORY WORKS'

ENDPASS DC.B 1

MSGFAIL DC.B 'MEMORY FAILS AT: '

ENDFAIL DC.B 1

READ DC.B 'Number Read: '

READEND DC.B 1

WRITE DC.B 'Number Written: '

WEND DC.B 1

BUFF DS.B 6

ORG $1000

START:

MOVE.L #$8B800,A5 ;Start of memory

MOVE.L #8BFFF,A6 ;End of memory

LOOP:

CMPA.L A5,A6 ;Check is A5 is at the end of the memory

BLT SET ;If yes, move to SET

MOVE.B #$AA,(A5)+ ;Else move $AA in memory, increment and loop again

BRA LOOP

SET:

MOVE.L #$8B800,A5 ;Reinitialize A5 to start of memory

TEST:

CMPI.B #$AA,(A5) ;Check if start of memory is $AA

BEQ PASS ;If yes, go to pass

BRA AA ;Else branch to AA

PASS:

MOVE.B #$55,(A5)+ ;Fill the memory with $55

CMPA.L A5,A6 ;Compare A5 and A6

BLT NEXTSET ;

BRA TEST

NEXTSET:

MOVE.L #$8B800,A5 ;Reinitialize A5 to start of memory

NEXTSTEP:

CMPI.B #$55,(A5) ;Check if A5 is $55

BEQ SECONDPASS ;If correct, branch to SECONDPASS

BRA F55 ;Else branch to F55

SECONDPASS:

MOVE.B #$AA,(A5)+ ;Check if A5 is $55 and increment value stored in A5

CMPA.L A5,A6 ;Compare A5 and A6

BLT OUTPUT ;

BRA NEXTSTEP ;

AA:

MOVE.L A5,D0 ;failed address

LEA MSGFAIL,A5 ;

LEA ENDFAIL,A6 ;

MOVE.B #243,D7 ;

TRAP #14 ;

LEA.L BUFF,A5 ;

LEA.L BUFF,A6 ;

CLR.L D1 ;

CLR.L D2 ;

MOVE.B #231,D7 ;

TRAP #14 ;

MOVE.B #243,D7 ;

TRAP #14 ;

LEA READ,A5 ;

LEA READEND,A6 ;

MOVE.B #243,D7 ;output number message

TRAP #14 ;

LEA.L BUFF,A5 ; adds 6 to next position

LEA.L BUFF,A6 ;

CLR.L D1 ;

CLR.L D2 ;

MOVE.B (A4),D0 ; get number

MOVE.B #233,D7 ; convert number to ascii

TRAP #14 ;

MOVE.B #243,D7 ; output number

TRAP #14 ;

LEA WRITE,A5 ;

LEA WEND,A6 ;

MOVE.B #243,D7 ; output number written

TRAP #14 ;

LEA.L BUFF,A5 ;

LEA.L BUFF,A6 ;

CLR.L D1 ;

CLR.L D2 ;

MOVE.W #$4141,$2200 ;

LEA $2200,A5 ;

LEA $2202,A6 ;

MOVE.B #243,D7 ;

TRAP #14 ;

BRA EXIT ;

F55:

MOVE.L A5,D0 ; get address of the failure

LEA MSGFAIL,A5 ; output fail 55

LEA ENDFAIL,A6 ;

MOVE.B #243,D7 ;

TRAP #14 ;

MOVE.L D0,A4 ; move back to address register

MOVE.B #231,D7 ; convert to ASCII

TRAP #14 ;

LEA.L BUFF,A5 ;

LEA.L BUFF,A6 ;

CLR.L D1 ;

CLR.L D2 ;

MOVE.B #243,D7 ;

TRAP #14 ;

LEA READ,A5 ;

LEA READEND,A6 ;

MOVE.B #243,D7 ; output number message

TRAP #14 ;

MOVE.B (A4),D0 ; get number

MOVE.B #233,D7 ; convert number to ascii

TRAP #14 ;

LEA.L BUFF,A5 ;

LEA.L BUFF,A6 ;

CLR.L D1 ;

CLR.L D2 ;

MOVE.B #243,D7 ;output number read

TRAP #14 ;

LEA WRITE,A5 ;

LEA WEND,A6 ;

MOVE.B #243,D7 ;output number written

TRAP #14 ;

MOVE.W #$3535,$2200 ;

LEA $2200,A5 ;

LEA $2203,A6 ;

MOVE.B #243,D7 ;

TRAP #14 ;

BRA EXIT ;

OUTPUT: LEA MSGPASS,A5

LEA ENDPASS,A6

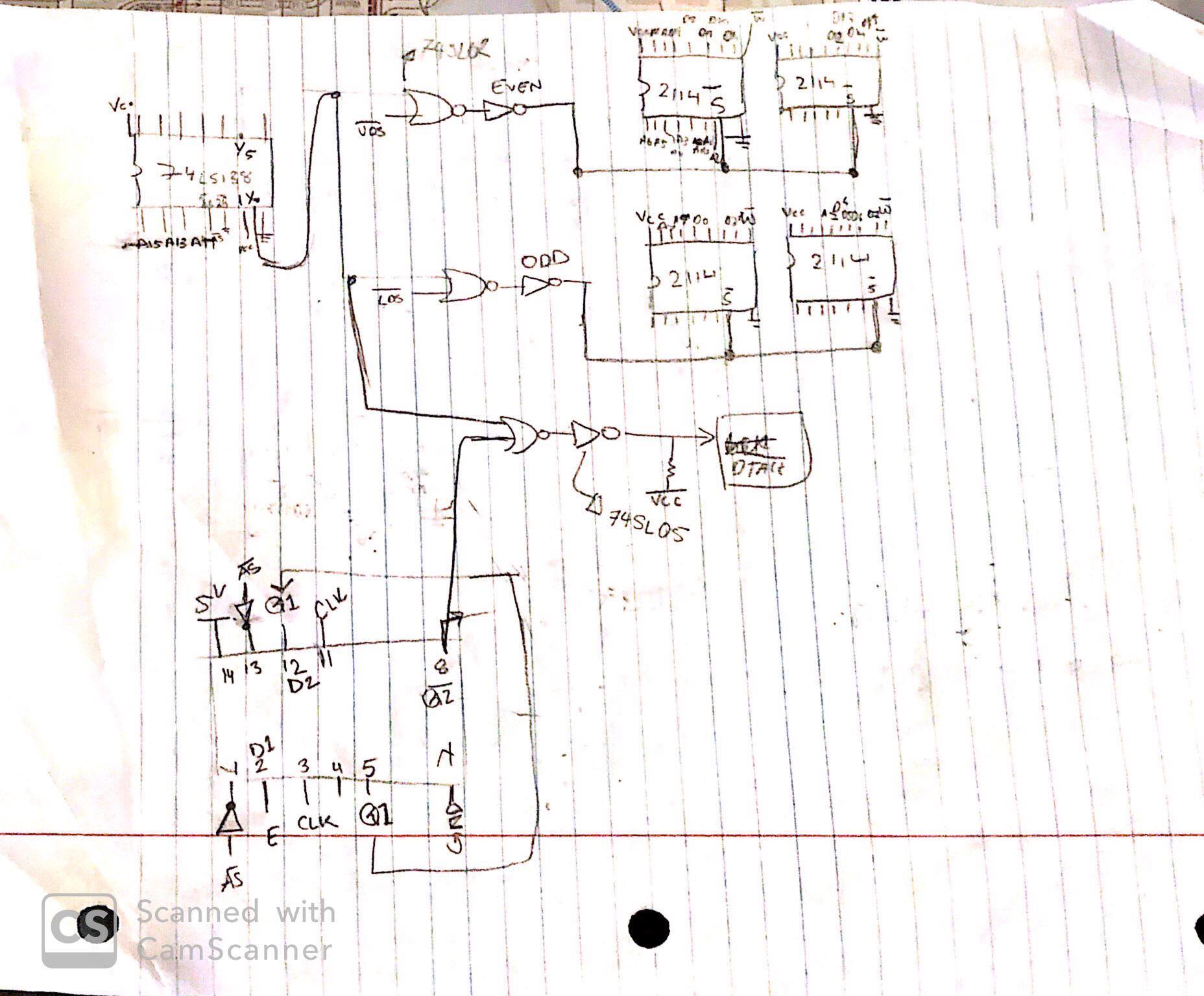
MOVE.B #243,D7 ;memory outputs pass

TRAP #14

EXIT: MOVE.B #228,D7 ;Return to SANPER

TRAP #14

Questions

1. **A schematic diagram of your hardware design.** 
2. **A fully commented listing of the memory test program.**

See discuss section.

1. **Discuss which address range you chose for the memory bank, and elaborate on the reasons for your selection.**

The chosen range is: is $8B800 to $8BFFF. It can accommodate 2K size of memory and it does not conflict with the memory space being used already by other devices. It selects the memory chips appropriately, since it uses A15 = 1, A13 = 1, and A11 = 1.

1. **Discuss the reasons for implementing memory tests. What conditions are you actually testing the hardware for?**

The test checks for the following:

* 1. Correct data being stored
  2. Memory device retaining data
  3. The ability to read back correctly stored data
  4. Data transfer acknowledgement

0xAA tests the even bits of the byte, and 0x55 sets all the odd bits to 1 and clears the even bits.

1. **Suggest some other bit patterns that could be used in a memory test program, and explain the reasons for your selections.**

Using 0x00FF and 0xFF00 in a memory test program would test the even and odd bytes. This would confirm that the implementation of UDS and LDS signal is successful.

1. **List the advantages and disadvantages of using Static RAMs over other types of memory devices such as EPROMS, Dynamic RAMs, etc.**

Advantage:

SRAM is composed of 6 transistors which does not need to be refreshed to keep its data.

SRAM operates faster.

SRAM is multipurpose.

Disadvantage:

SRAM is volatile and will lose all its data if the power is turned off. Using EPROMS would solve this issue since it keeps its data even when the power is turned off.

SRAM is also more expensive than other memory chip.

**IV. Conclusions**

Students were able to build a circuit that could transfer data to and from the SANPER unit’s bus. One lesson the students learn is to debug the circuit step by step instead of building the whole design and then trying to debug it. Unfortunately, one of the SRAM chips was defective which caused issues in transferring data. Had the students debugged the circuit step by step, this issue would have been found easier. Overall, the group was able to understand the principle behind memory design and came up with a solid design which works perfectly theoretically.

**References**

[1] Experiment 4 Lab Manual